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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/621,614	07/21/2000	Yasuyuki Morishita	040373/0287	4521

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/621,614	MORISHITA, YASUYUKI	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA) in view of Watt (5,701,024).

APA teaches in figure 7 a semiconductor device having, on a semiconductor substrate 20, an input/output protection circuit section that contains a complementary N type field effect transistor wherein the complementary field effect transistor comprises a first field effect transistor having a first 3c and second 3b diffusion layers of first conductive type, respectively, and a gate electrode 6 that is disposed between these layers and a second field effect transistor having a third 4c and fourth 4b diffusion layers of second conductive type, respectively, and a gate electrode 5 that is disposed between these layers, wherein a first dopant diffusion region 4a of second conductive type is set at a distance from the first field effect transistor, and a second dopant diffusion region 3a of first conductive type is set at a distance from the second field effect transistor, wherein the first dopant diffusion region 4a is connected to a first reference potential Vss, the

second dopant diffusion region 3a is connected to a second reference potential Vdd, and the second diffusion layer 3b and the fourth diffusion layer 4b are each connected to an input/output terminal section 7.

APA does not teach a first conductive type well under the first diffusion layer, having a lower dopant concentration than the first diffusion layer.

Watt teaches in figure 5 a first conductive type well 54 under the first diffusion layer 44, having a lower dopant concentration than the first diffusion layer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first conductive type well under the first diffusion layer, having a lower dopant concentration than the first diffusion layer in APA's device in order to reduce contact spiking during ESD event. The combination is motivated by the teachings of Watt who points out the advantages of using a first conductive type well under the first diffusion layer.

Regarding claim 1, APA teaches in figures 14-15 and related text that an input/output protection circuit generally composed of a plurality of field effect transistors connected in parallel, each of which has a first and second diffusion layers of first conductive type.

Regarding claims 2, 5 and 6, APA teaches a gate electrode of the first field effect transistor and the first dopant diffusion region are placed over the second conductive

type well that is formed on the surface of the semiconductor substrate. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the bottom of the first conductive type well at the same depth as the bottom of the second conductive type well or at a level deeper than the bottom of the second conductive type well in APA's device in order to increase the distance that a spike can propagate without shorting out the junction.

Regarding claim 6, APA teaches a dopant high-concentration region 20 beneath the second conductive type well, and containing second conductive type dopants with a higher dopant concentration than the second conductive type well.

3. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA) in view of Watt (5,701,024) and Morihisa (JP 10-173070). APA teaches in figure 7 a semiconductor device having, on a semiconductor substrate 20, an input/output protection circuit section that contains a complementary N type field effect transistor wherein the complementary field effect transistor comprises a first field effect transistor having a first 3c and second 3b diffusion layers of first conductive type, respectively, and a gate electrode 6 that is disposed between these layers and a second field effect transistor having a third 4c and fourth 4b diffusion layers of second conductive type, respectively, and a gate electrode 5 that is disposed between these

layers, wherein a first dopant diffusion region 4a of second conductive type is set at a distance from the first field effect transistor, and a second dopant diffusion region 3a of first conductive type is set at a distance from the second field effect transistor, wherein the first dopant diffusion region 4a is connected to a first reference potential Vss, the second dopant diffusion region 3a is connected to a second reference potential Vdd, and the second diffusion layer 3b and the fourth diffusion layer 4b are each connected to an input/output terminal section 7.

APA does not teach a first conductive type well under the first diffusion layer, having a lower dopant concentration than the first diffusion layer.

Watt teaches in figure 5 a first conductive type well 54 under the first diffusion layer 44, having a lower dopant concentration than the first diffusion layer. Morihisa teaches in figure 2 a first conductive type well 5' under the first diffusion layer 16, wherein the bottom of the first conductive type well 5' is at the same depth as the bottom of the second conductive type well 5 or at a level deeper than the bottom of the second conductive type well, and having a lower dopant concentration than the first diffusion layer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first conductive type well under the first diffusion layer, having a lower dopant concentration than the first diffusion layer in APA's device in order to reduce contact spiking during ESD event. The combination is motivated by the

teachings of Watt who points out the advantages of using a first conductive type well under the first diffusion layer.

Regarding claim 1, APA teaches in figures 14-15 and related text that an input/output protection circuit generally composed of a plurality of field effect transistors connected in parallel, each of which has a first and second diffusion layers of first conductive type.

Regarding claims 2, 5 and 6, APA teaches a gate electrode of the first field effect transistor and the first dopant diffusion region are placed over the second conductive type well that is formed on the surface of the semiconductor substrate. Morihisa teaches in figure 2 a bottom of the first conductive type well 5' is at the same depth as the bottom of the second conductive type well 5 or at a level deeper than the bottom of the second conductive type well. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the bottom of the first conductive type well at the same depth as the bottom of the second conductive type well or at a level deeper than the bottom of the second conductive type well in APA's device in order to increase the distance that a spike can propagate without shorting out the junction.

Regarding claim 6, APA teaches a dopant high-concentration region 20 beneath the second conductive type well, and containing second conductive type dopants with a higher dopant concentration than the second conductive type well.

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA) in view of Yamamoto (5,898,206) or Morihisa (JP 10-173070).

APA teaches substantially the entire claimed structure, as applied to claims 1 and 4 above, except a first conductive type well under the first diffusion layer, and at least partially under an element isolation film, having a lower dopant concentration than the first diffusion layer.

Yamamoto teaches in figure 10a a first conductive type well 21a under the first diffusion layer 3A, and at least partially under an element isolation film 12A, having a lower dopant concentration than the first diffusion layer. Morihisa teaches in figure 2 a first conductive type well 5' under the first diffusion layer 16, and at least partially under an element isolation film 30, wherein the bottom of the first conductive type well 5' is at the same depth as the bottom of the second conductive type well 5 or at a level deeper than the bottom of the second conductive type well, and having a lower dopant concentration than the first diffusion layer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first conductive type well under the first diffusion layer, and at least partially under an element isolation film,

having a lower dopant concentration than the first diffusion layer in APA's device in order to reduce contact spiking during ESD event and in order to improve the breakdown characteristics of the device. The combination is motivated by the teachings of Yamamoto who point out the advantages of using a first conductive type well in the location depicted in figure 10a.

Response to Arguments

5. Applicant argues on page 5 that Watt does not teach a first conductivity type well should never be connected to an input terminal.

In response to applicant's argument Watt does not teach a first conductivity type well should never be connected to an input terminal, it is noted that these features are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

6. Applicant argues on page 6 that Watt does not teach a first diffusion region connected to ground.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections

are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). APA teaches substantially the entire claimed structure, including a first diffusion region connected to ground. Watt is not cited to teach a first diffusion region connected to ground. Watt is cited to teach a first conductive type well under the first diffusion layer, having a lower dopant concentration than the first diffusion layer.

7. Applicant argues on pages 6-7 that Watt uses the first conductive type well to prevent spiking, whereas applicant uses the first conductive type well to raise the electric potential of an adjacent base region.

In response to applicant's argument that Watt uses the first conductive type well for reasons different than those of applicant, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 3 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772.**

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Ori Nadav

March 12, 2002